BUK9875-100A

N-channel TrenchMOS logic level FET

Rev. 02 — 31 May 2010 | Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for logic level gate drive sources

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

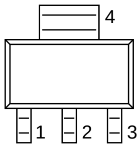
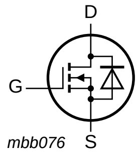
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 150$ °C	-	-	100	V
I_D	drain current	$V_{GS} = 5$ V; $T_{sp} = 25$ °C; see Figure 1; see Figure 3	-	-	7	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; see Figure 2	-	-	8	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 8$ A; $T_j = 25$ °C	-	-	84	mΩ
		$V_{GS} = 10$ V; $I_D = 8$ A; $T_j = 25$ °C	-	62	72	mΩ
		$V_{GS} = 5$ V; $I_D = 8$ A; $T_j = 25$ °C; see Figure 12; see Figure 13	-	64	75	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 7$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	-	49	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **SOT223 (SC-73)**	
2	D	drain		
3	S	source		
4	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9875-100A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

4. Marking

Table 4. Marking codes

Type number	Marking code[1]
BUK9875-100A	987510A

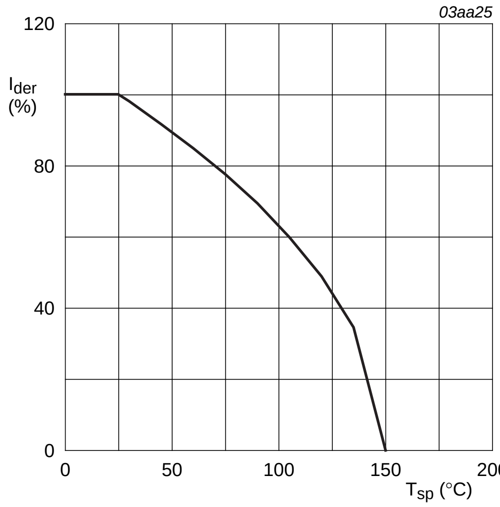
[1] % = -: made in Hong Kong; % = p: made in Hong Kong; % = t: made in Malaysia; % = W: made in China

5. Limiting values

Table 5. Limiting values

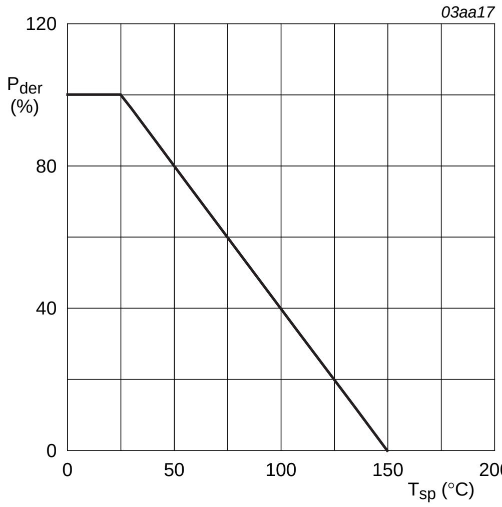
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 150 °C	-	-	100	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ	-	-	100	V
V_{GS}	gate-source voltage		-10	-	10	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 5 V; see Figure 1; see Figure 3	-	-	7	A
		T_{sp} = 100 °C; V_{GS} = 5 V; see Figure 1	-	-	4	A
I_{DM}	peak drain current	T_{sp} = 25 °C; t_p ≤ 10 µs; pulsed; see Figure 3	-	-	28	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 2	-	-	8	W
T_{stg}	storage temperature		-55	-	150	°C
T_j	junction temperature		-55	-	150	°C
V_{GSM}	peak gate-source voltage	pulsed; t_p ≤ 50 µs	-15	-	15	V
Source-drain diode						
I_S	source current	T_{sp} = 25 °C	-	-	7	A
I_{SM}	peak source current	t_p ≤ 10 µs; pulsed; T_{sp} = 25 °C	-	-	28	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 7 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	49	mJ



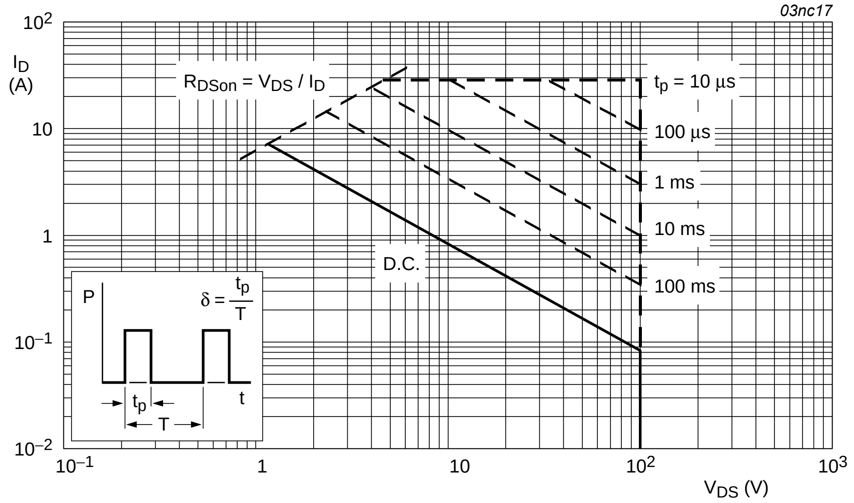
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{amb} = 25°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	see Figure 4	-	70	-	K/W

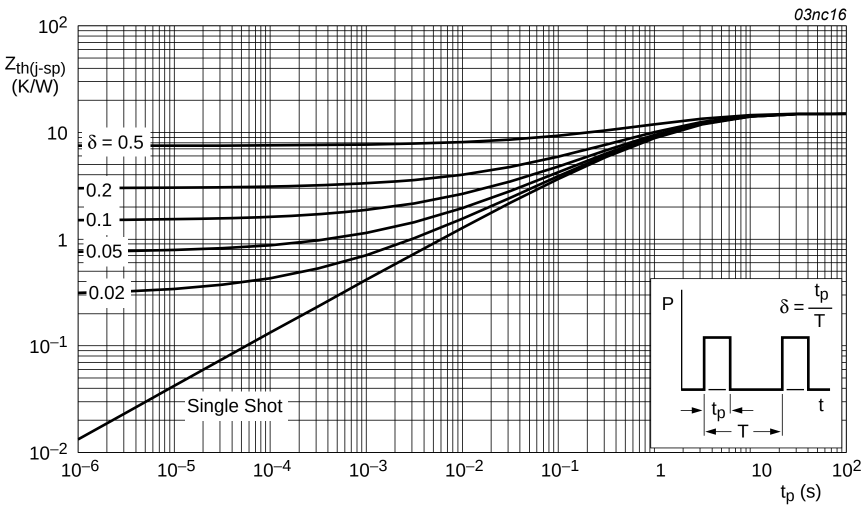
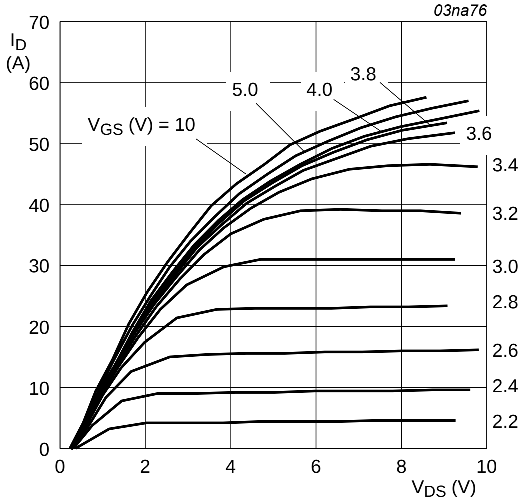


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

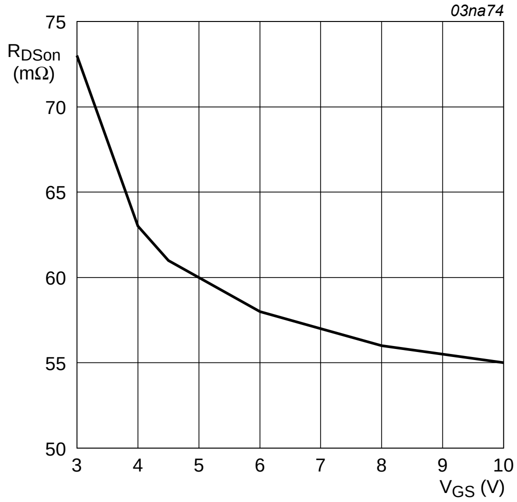
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11	1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11	-	-	2.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 °C; see Figure 11	0.6	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	10	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 150 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -10 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 8 A; T_j = 150 °C; see Figure 12; see Figure 13	-	-	162	mΩ
		V_{GS} = 4.5 V; I_D = 8 A; T_j = 25 °C	-	-	84	mΩ
		V_{GS} = 10 V; I_D = 8 A; T_j = 25 °C	-	62	72	mΩ
		V_{GS} = 5 V; I_D = 8 A; T_j = 25 °C; see Figure 12; see Figure 13	-	64	75	mΩ
Dynamic characteristics						
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 14	-	1270	1690	pF
C_{oss}	output capacitance		-	140	167	pF
C_{rss}	reverse transfer capacitance		-	90	124	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	13	-	ns
t_r	rise time		-	120	-	ns
$t_{d(off)}$	turn-off delay time		-	58	-	ns
t_f	fall time		-	57	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	63	-	ns
Q_r	recovered charge		-	220	-	nC



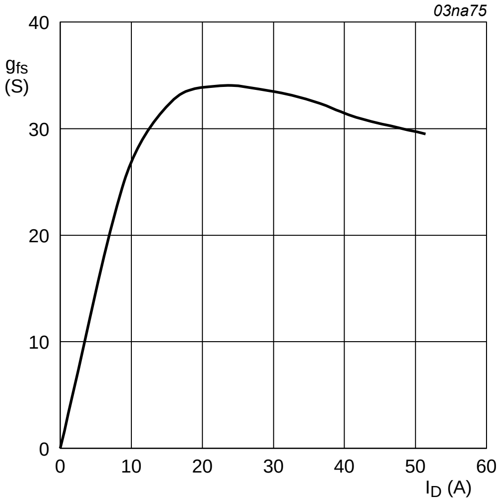
$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



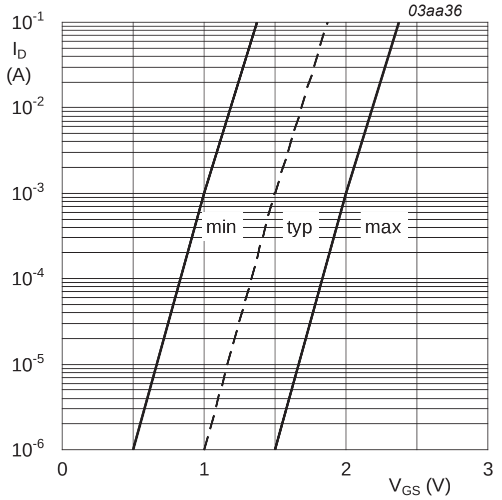
$T_j = 25°C; I_D = 8A$

Fig 6. Drain-source on-state resistance as a function of gate-source; typical values



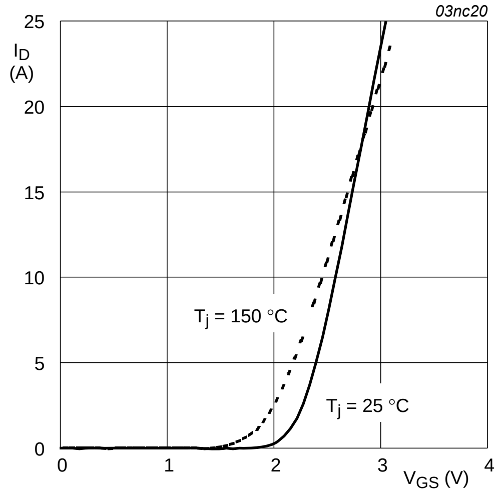
$T_j = 25°C; V_{DS} = 25V$

Fig 7. Forward transconductance as a function of drain current; typical values



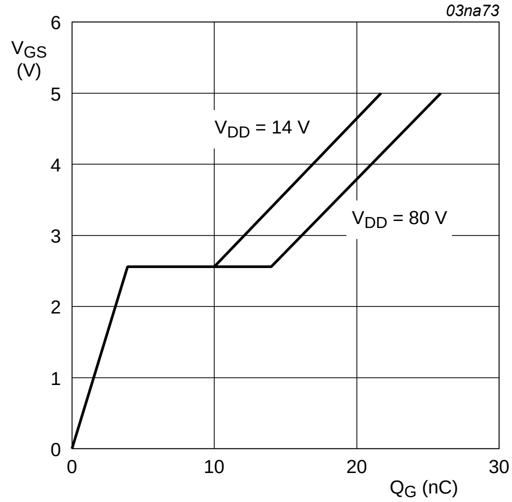
$T_j = 25°C; V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



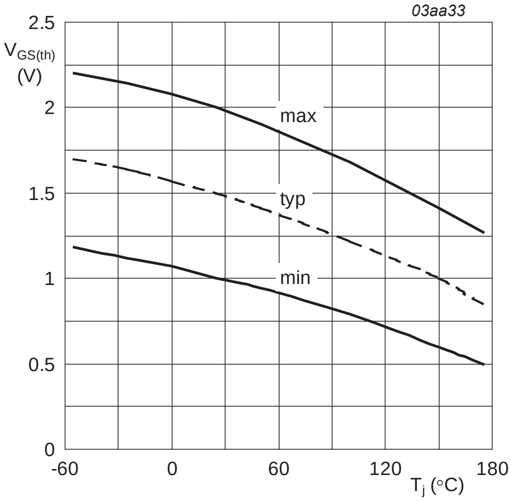
$V_{DS} = 25V$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



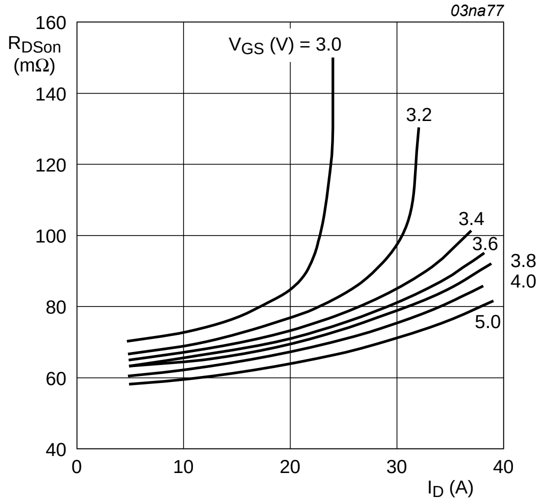
$T_j = 25°C; I_D = 20A$

Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values



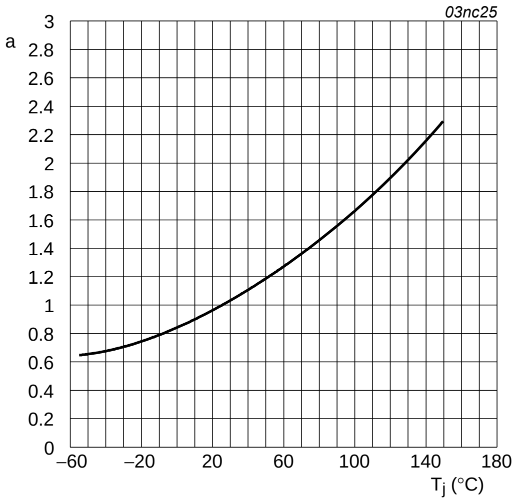
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



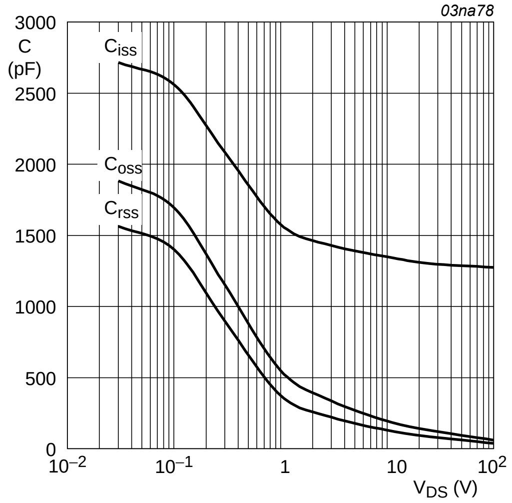
$T_j = 25°C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



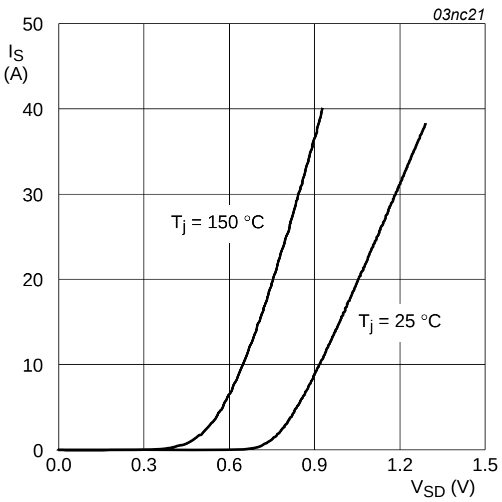
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



$$V_{GS} = 0V; f = 1MHz$$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

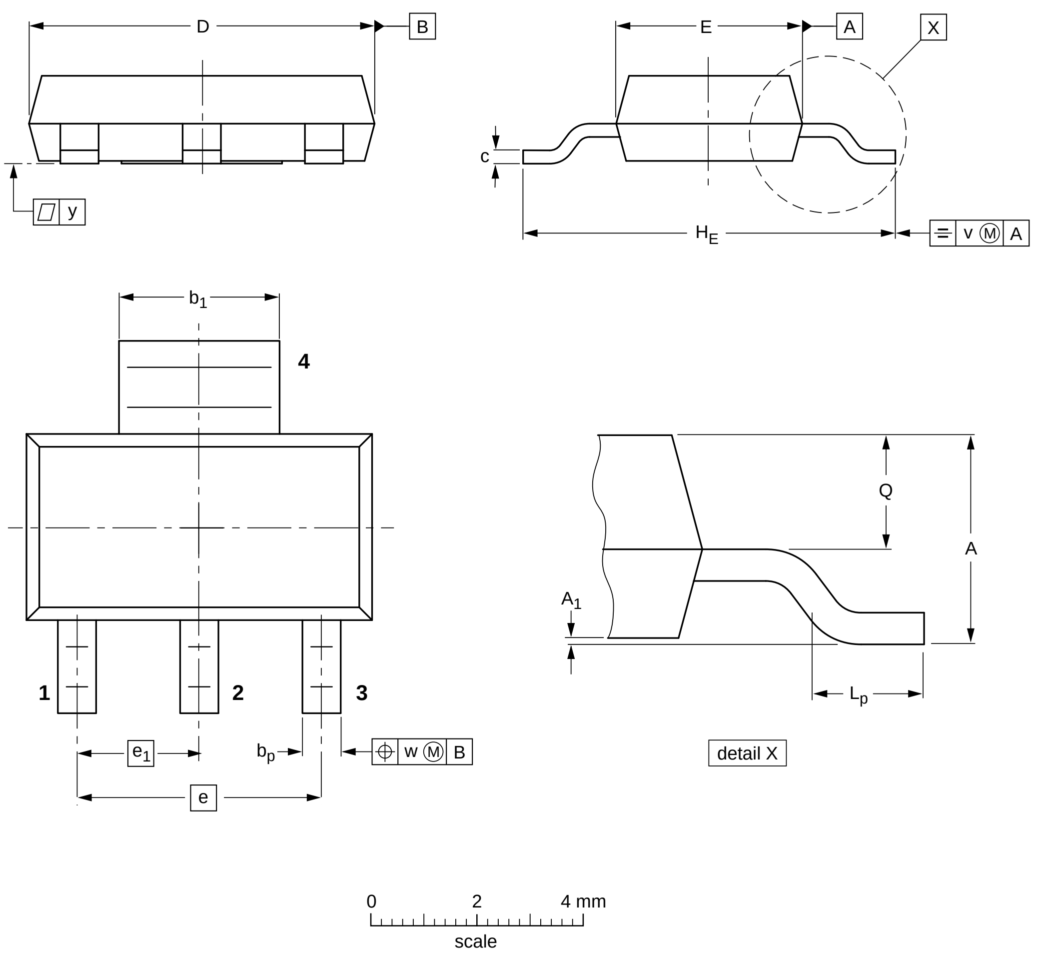


$$V_{GS} = 0V$$

Fig 15. Reverse diode current as a function of reverse diode voltage; typical values

8. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig 16. Package outline SOT223 (SC-73)

9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9875-100A v.2	20100531	Product data sheet	-	BUK9875-100A-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUK9875-100A-01 (9397 750 07735)	20010130	Product specification	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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